

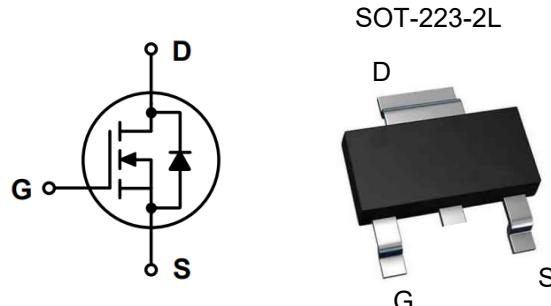
Description

The CM65R380PS32 is the N-Channel enhancement mode power field effect transistors with high cell density, high voltage Super Junction technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

Features

- V_{DS}: 650V
- I_D: 7.9A
- R_{DS(on)} (@V_{GS}=10V) : < 380mΩ
- High density cell design for extremely low R_{DS(on)}
- Excellent on-resistance and DC current capability

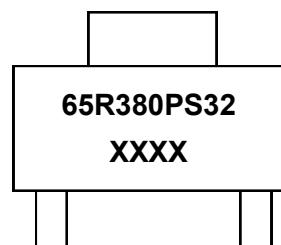
Equivalent Circuit and Pin Configuration



Applications

- Cellular Handsets and Accessories
- Personal Digital Assistants
- Portable Instrumentation
- Load switch

Marking Information



Device Code = 65R380PS32
Date Code = XXXX

Ordering Information

Part Number	Packaging	Reel Size
CM65R380PS32	4000/Tape & Reel	13 inch

Absolute Maximum Ratings (T_A=25 °C unless otherwise noted)

Parameter	Symbol	Maximum	Unit
Drain-source Voltage	V _{DS}	650	V
Gate-source Voltage	V _{GS}	±30	V
Continuous Drain Current ⁽¹⁾	I _D	7.9	A
T _c =100°C		5.0	
Pulsed Drain Current ⁽²⁾	I _{DM}	32	A
Total Power Dissipation	P _D @ T _c =25°C	54	W
	Derating Factor above 25°C	0.43	W/°C
Thermal Resistance Junction-to-Solder Case ⁽³⁾	R _{θJC}	2.3	°C/W
Thermal Resistance Junction-to-Solder Point ⁽³⁾	R _{θJS}	18	°C/W
Thermal Resistance Junction-to-Ambient ⁽³⁾	R _{θJA}	75	°C/W
Junction and Storage Temperature Range	T _{J,TSTG}	-55 to +150	°C

Electrical Characteristics (T_J=25 °C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BVDSS	V _{GS} =0V, I _D =250µA	650			V
Zero Gate Voltage Drain Current	I _{DSS}	V _D S=650V, V _{GS} =0V, T _C =25°C			1	µA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±30V, V _D S=0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _D S=V _{GS} , I _D =250µA	2.5		4.5	V
Static Drain-Source on-Resistance	R _D S(on)	V _{GS} =10V, I _D =4A		325	380	mΩ
Diode Forward Voltage	V _{SD}	I _S =7.9A, V _{GS} =0V		0.9	1.2	V
Maximum Body-Diode Continuous Current	I _S				7.9	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _D S=400V, V _{GS} =0V, f=250KHz		624		pF
Output Capacitance	C _{oss}			17		
Reverse Transfer Capacitance	C _{rss}			3.6		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _D S=400V, I _D =4A		16.5		nC
Gate Source Charge	Q _{gs}			4.6		
Gate Drain Charge	Q _{gd}			8.8		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =50V, I _D =4A, R _{GEN} =10Ω		39		ns
Turn-on Rise Time	t _r			17.6		
Turn-off Delay Time	t _{D(off)}			46		
Turn-off Fall Time	t _f			20.8		

Noted: (1) Limited by T_{j,max}. Maximum Duty Cycle D = 0.50; DPAK / IPAK equivalent.

(2) Pulse width t_p limited by T_{j,max}

(3) Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70µm thickness) copper area for drain connection and cooling.

Typical Performance Characteristics

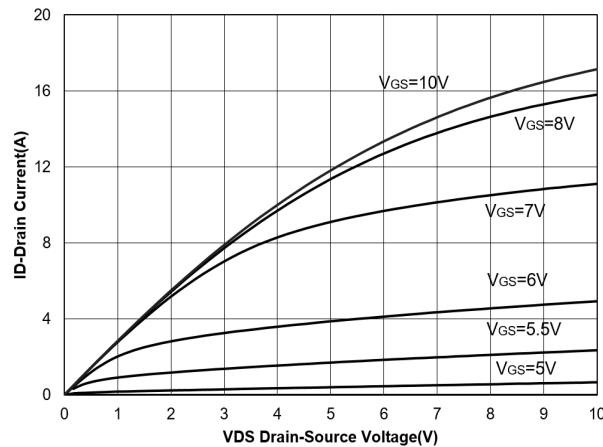


Figure 1. Output Characteristics

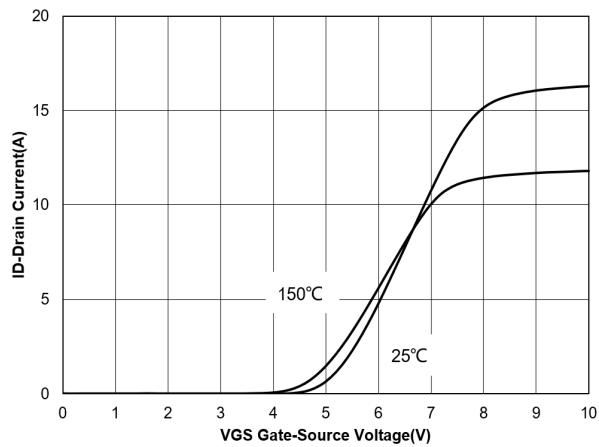


Figure 2. Transfer Characteristics

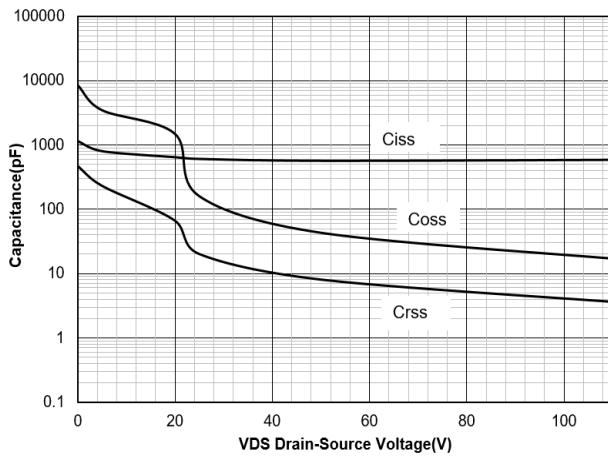


Figure 3. Capacitance Characteristics

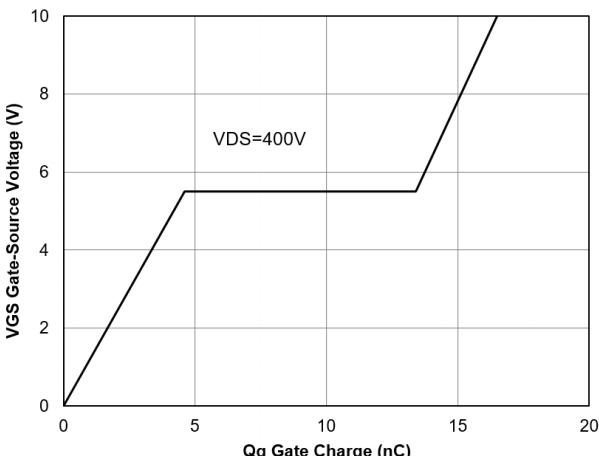


Figure 4. Gate Charge

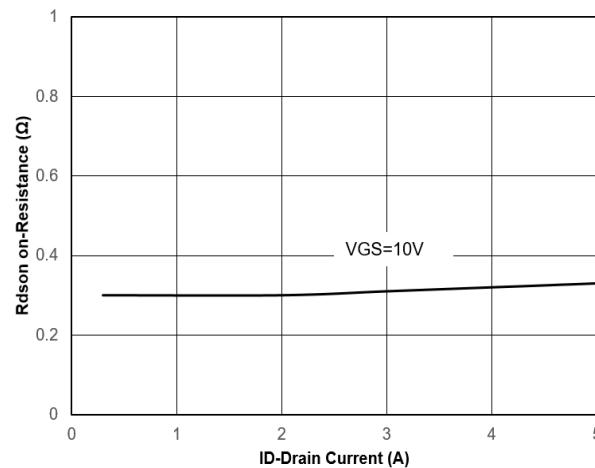


Figure 5. Drain-Source on Resistance

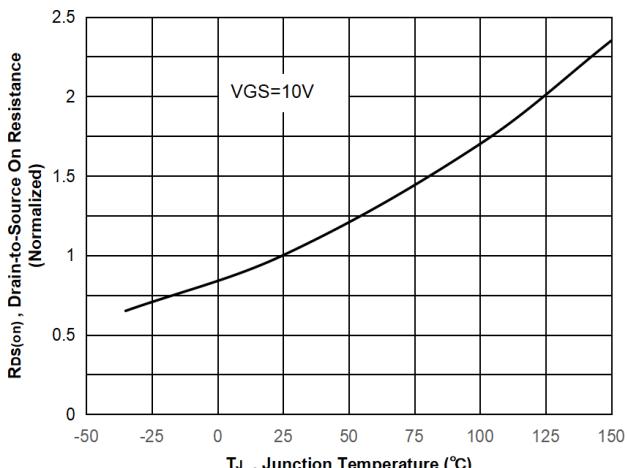


Figure 6. Normalized On-Resistance
Vs. Temperature

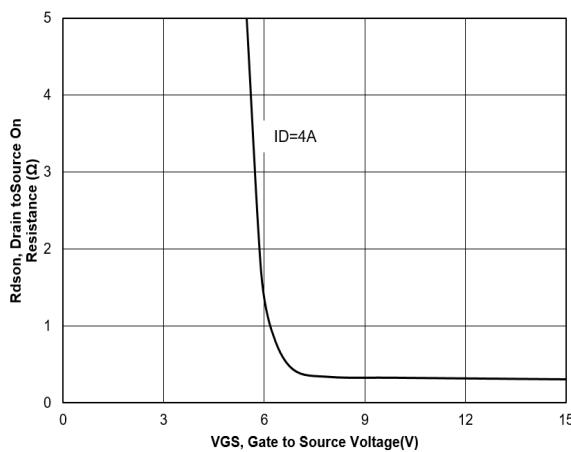


Figure 7. Typical Drain to Source ON Resistance
VS Gate Voltage and Drain Current

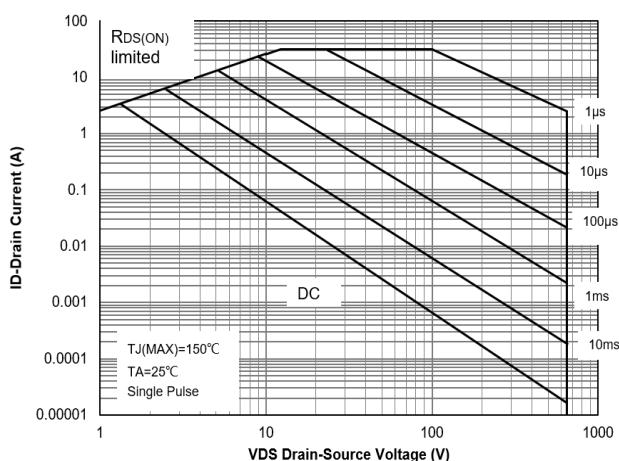


Figure 8. Safe Operation Area

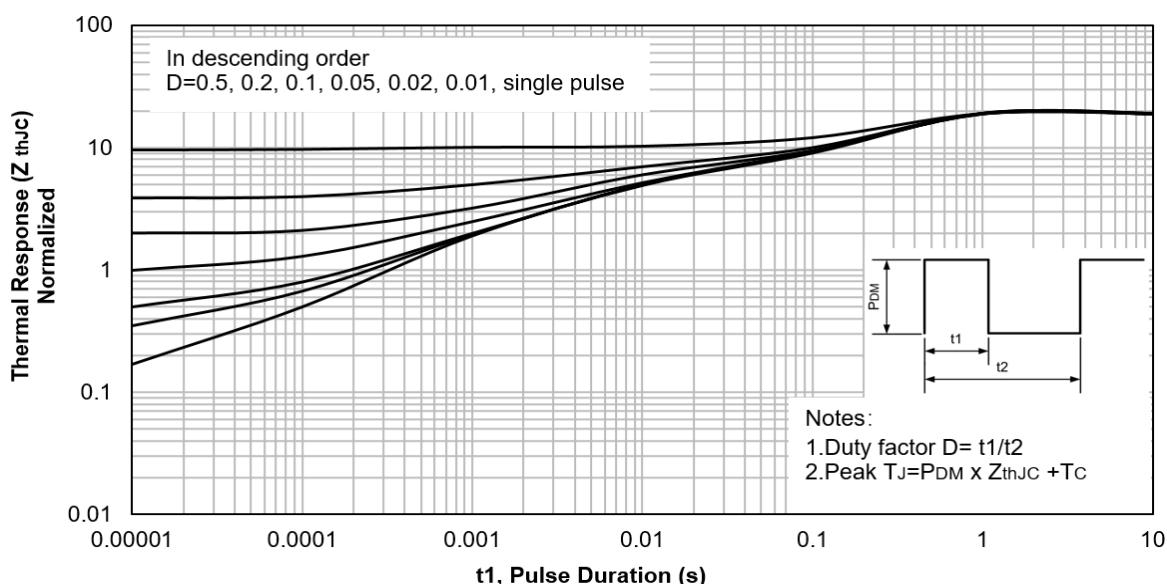


Figure 9. Maximum Effective Transient Thermal Impedance ,Junction-to-Ambient

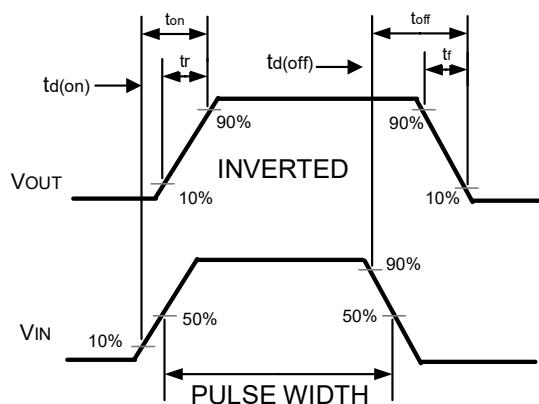
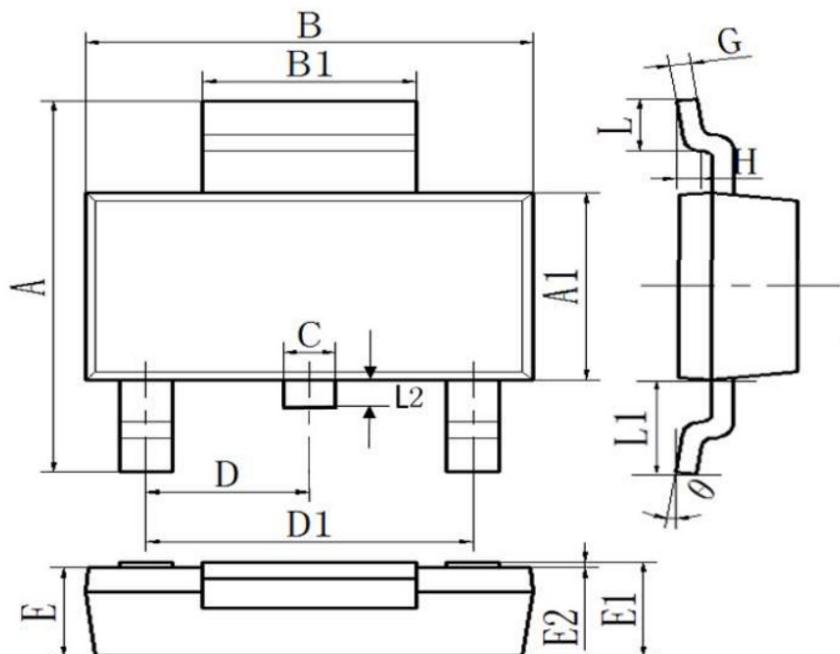


Figure 10. Switching wave

SOT-223-2L Package Outline Drawing



符号	标准	下公差	上公差	下限值	上限值
A	7.0	-0.2	0.2	6.8	7.2
A1	3.5	-0.1	0.1	3.4	3.6
B	6.5	-0.2	0.2	6.3	6.7
B1	3.05	-0.1	0.1	2.95	3.15
C	0.74	-0.08	0.08	0.66	0.82
D	2.3	-0.05	0.05	2.25	2.35
D1	4.6	-0.1	0.1	4.5	4.7
E	1.6	-0.15	0.15	1.45	1.75
E1	1.66	-0.15	0.15	1.51	1.81
E2	0.08	-0.06	0.06	0.02	0.14
G	0.3	-0.05	0.05	0.25	0.35
H	0.25	-0.05	0.05	0.20	0.30
L	0.95	-0.2	0.2	0.75	1.15
L1	1.75	-0.1	0.1	1.65	1.85
L2	0.5REF				
θ	8	-4	4	0	8

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